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EXAMINER	
AHMED, ENAM	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/757,182	BAIG ET AL.	
	Examiner	Art Unit	
	Enam Ahmed	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *5/20/05, 4/12/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Non-Final Rejection

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-6 and 8-10 are rejected under 35 U.S.C. 102(b) as being unpatentable over Ransijn (U.S. Patent No. 6,275,959).

With respect t claim 1, the Ransijn reference teaches receiving sais signal (column 1, line 67); comparing a portion of said signal to a signal – eye (column 2, lines 3-5); determining said logical data based upon said comparing (column 2, lines 5 – 14); determining said timing distortions of said portion (column 5, lines 59 – column 6, line 6); centering said signal – eye with respect to said portion based upon said determined timing distortions (column 1, lines 23-51).

With respect to claim 2, the Ransijn reference teaches wherein said comparing comprises comparing voltage threshold to said portion (column 1, lines 13-16).

With respect to claim 3, the Ransijn reference teaches wherein said centering said signal – eye comprises adjusting aid voltage threshold (column 1, lines 23-31).

With respect to claim 4, the Ransijn reference teaches wherein said comparing further comprises comparing a current threshold to said portion (column 7, lines 15-48).

With respect to claim 5, the Ransijn reference teaches wherein said centering said signal – eye comprises adjusting said current threshold (column 7, lines 50-65).

With respect to claim 6, the Ransijn reference teaches wherein said centering said signal – eye comprises adjusting the voltage of said portion (column 3, lines 57-60), (column 4, 18-39).

With respect to claim 8, the Ransijn reference teaches wherein said centering said signal – eye comprises adjusting the current of said portion (column 1, lines 22 – 51).

With respect to claim 9, the Ransijn reference teaches wherein said portion is a bit of said logical data is defined by a positive signal component and a negative signal component and an average of said positive signal component and negative signal is compared to said signal – eye (column 1, lines 8-21).

With respect to claim 10, the Ransijn reference teaches wherein said determining said distortions comprises performing a bit – error – rate analysis on said signal (see Fig. 4, BER).

Claims 12-28 are rejected under 35 U.S.C. 102(b) as being unpatentable over Wiatrowski et al. (U.S. Patent No. 5,521,941).

With respect to claim 12, the Wiatrowski et al. reference teaches a communication channel providing said signal (column 1, lines 1-24); a clock and data recovery decision circuit, coupled to said communication channel, for determining the logical data included in the said signal,l wherein said signal – eye is compared to an average value of said signal (column 2, lines 11-20), (see Fig. 1, Clock Recovery – 105, Signal Recovery and Processing – 109); and a threshold adjust block, coupled to said communication channel, for providing symmetry between said signal and said signal – eye (Automatic Threshold Adjustment Circuitry – 107).

With respect to claim 13, the Wiatrowski et al. reference teaches wherein said signal – eye is a voltage threshold (column 1, lines 24-44).

With respect to claim 14, the Wiatrowski et al. reference teaches wherein said threshold adjust block adjusts said voltage threshold (column 2, lines 27-35).

With respect to claim 15, the Wiatrowski et al. reference teaches wherein said signal – eye is a current threshold (column 3, lines 12 – 29).

With respect to claim 16, the Wiatroski et al. reference teaches wherein said threshold adjust block adjusts said current threshold (column 3, lines 37-62).

With respect to claim 17, the Wiatrowski et al. reference teaches wherein said threshold adjust block adjusts the voltage of said signal on said communication channel (column 2, lines 21-35).

With respect to claim 18, the Wiatrowski et al. reference teaches wherein said threshold adjust block decreases the voltage of said signal on said communication channel (column 2, lines 36-57).

With respect to claim 19, the Wiatrowski et al. reference teaches wherein said threshold adjust block decreases the voltage of said signal by sinking current from said communication channel (column 6, lines 2-27).

With respect to claim 20, the Wiatrowski et al. reference teaches comprising a distorted signal detector coupled to said communications channel for detecting distortions in said signal (column 1, lines 16-24), (column 1, lines 36-44).

With respect to claim 21, the Wiatrowski et al. reference teaches wherein said distorted signal detector performs a bit-error-rate analysis of said logical data to detect said distortions (column 2, line 58-column 3, line 11).

With respect to claim 22, the Wiatrowski et al. reference teaches wherein said distorted signal detector compares a peak voltage of said signal to an ideal peak voltage for said signal to detect said distortions (column 4, lines 31 – 63).

With respect to claim 23, the Wiatrowski et al. reference teaches wherein said distorted signal detector is coupled to said threshold adjust block and controls the operation of said threshold adjust block (column 2, lines 36-57).

With respect to claim 24, the Wiatrowski et al. reference teaches comprising a programmable logic device coupled to said clock and data recovery circuit wherein said programmable logic device receives the logical data included in said signal (column 6, line 66-column 7, line 70

With respect to claim 25, the Wiatrowski et al. reference teaches a communication channel providing said signal (column 1, lines 1-23); a threshold adjust block, coupled to said communication channel, for providing symmetry between said signal and said signal – eye, wherein said threshold adjust block adjusts said signal – eye by adjusting the amount of current in said signal (see Fig. 1, Automatic Threshold Adjustment circuitry - 107).

With respect to claim 26, the Wiatrowski et al. reference teaches wherein said threshold adjust block sinks current from said signal (column 3, lines 25-34).

With respect to claim 27, the Wiatrowski et al. reference teaches a clock and data recovery decision circuit (see Fig. 1, Clock Recovery – 105 and Signal recovery and processing – 109); coupled to said communication channel, for determining the logical data included in said signal (column 1, lines 1 – 24); wherein said signal – eye is compared to an average value of said signal (column 1, lines 24-44).

With respect to claim 28, the Wiatrowski et al. reference teaches comprising a programmable logic device coupled to said clock and data recovery circuit wherein said programmable logic device receives the logical data included in said signal (column 6, line 66-column 7, line 70).

35 U.S.C. 103 Rejection

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 7 is rejected over Ransijn (U.S. Patent No. 6,275,959) further in view of Wiatrowski et al. (U.S. Patent No. 5,521,941).

With respect to claim 7, the Ransijn reference teaches all of the limitations of claim 6. The Ransijn reference does not teach wherein adjusting the voltage of said portion comprises sinking the current of said portion. The Wiatrowski et al. reference teaches wherein adjusting the voltage of said portion comprises sinking the current of said portion (column 2, lines 36-57). Thus it would have been obvious to one of ordinary skill in the art to have combined the references Ransijn and Wiatrowski et al. to have wherein adjusting the voltage of said portion comprises sinking the current of said portion. The motivation for wherein adjusting the voltage of said portion comprises sinking the current of said portion is for accurate symbol recovery for multi – level signals.

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ransijn (U.S. Patent No. 6,275,959) further in view of Wiatrowski et al. (U.S. Patent No. 5,521,941).

With respect to claim 11, the Ransijn reference teaches all of the limitations of claim 1. The Ransijn reference does not teach wherein said determining said distortions comprises comparing a peak voltage for said portion to an ideal peak voltage for said portion. The Wiatrowski et al. reference teaches determining said distortions comprises comparing a peak voltage for said portion to an ideal peak voltage for said portion (column 4, lines 31-63). Thus it would have been obvious to one of ordinary skill in the art to have combined the references Ransijn and Wiatrowski et al. to incorporate determining said distortions comprises comparing a peak voltage for said portion to an ideal peak voltage for said portion into the claimed invention. The motivation for

determining said distortions comprises comparing a peak voltage for said portion to an ideal peak voltage for said portion is because the optimal threshold level is retained longer for better BER performance (column 6, lines 5-6 – Wiatrowski et al. reference).

Claims 29-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wiatrowski et al. (U.S. Patent No. 5,521,941) further in view of Hadjihassan et al. (U.S. Patent No. 6,871,304).

With respect to claim 29, the Wiatrowski et al. reference teaches all of the limitations of claim 25. The Wiatrowski et al. reference does not teach wherein said threshold adjust block is operable to adjust the current of said signal at a plurality of current amounts. The Hadjihassan et al. reference teaches wherein said threshold adjust block is operable to adjust the current of said signal at a plurality of current amounts (column 5, lines 51 – 59). Thus it would have been obvious to have combined the references Wiatrowski et al. and Hadjihassan et al. to incorporate wherein said threshold adjust block is operable to adjust the current of said signal at a plurality of current amounts. The motivation for wherein said threshold adjust block is operable to adjust the current of said signal at a plurality of current amounts is to approach optimum values of the slicing parameters rapidly without causing large variations in the BER (column 3, lines 56 – 58 – Hadjihassan et al. reference).

With respect to claim 30, all of the limitations of claim 29 have been addressed above. The Wiatrowski et al. reference does not teach comprising a plurality of control signals having a plurality of control signals having a plurality of logical combinations,

wherein at least one of said plurality of logical combinations sinks current from said signal by one of said plurality of current amounts. The Hadjihassan et al. reference teaches comprising a plurality of control signals having a plurality of control signals having a plurality of logical combinations, wherein at least one of said plurality of logical combinations sinks current from said signal by one of said plurality of current amounts (column 6, lines 3 – 22). Thus it would have been obvious to one of ordinary skill in the art to have combined the references Wiatrowski et al. and Hadjihassan et al. to have incorporated a plurality of control signals having a plurality of control signals having a plurality of logical combinations, wherein at least one of said plurality of logical combinations sinks current from said signal by one of said plurality of current amounts into the claimed invention. The motivation for a plurality of control signals having a plurality of control signals having a plurality of logical combinations, wherein at least one of said plurality of logical combinations sinks current from said signal by one of said plurality of current amounts is for wherein said threshold adjust block is operable to adjust the current of said signal at a plurality of current amounts is to approach optimum values of the slicing parameters rapidly without causing large variations in the BER (column 3, lines 56 – 58 – Hadjihassan et al. reference).

With respect to claim 31, all of the limitations of claim 29 have been addressed above. The Wiatrowski et al. reference does not teach a plurality of control signals having a plurality of logical combinations, wherein at least one of said plurality of logical combinations increases current from said signal by one of said plurality of current amounts. The Hadjihassan et al. reference teaches a plurality of control signals having a plurality of logical combinations, wherein at least one of said plurality of logical

combinations increases current from said signal by one of said plurality of current amounts (column 6, lines 14-22). Thus it would have been obvious to one of ordinary skill in the art to have combined the references Wiatrowski et al. and Hadjihassan et al. to incorporate a plurality of control signals having a plurality of logical combinations, wherein at least one of said plurality of logical combinations increases current from said signal by one of said plurality of current amounts into the claimed invention. The motivation for a plurality of control signals having a plurality of logical combinations, wherein at least one of said plurality of logical combinations increases current from said signal by one of said plurality of current amounts is to approach optimum values of the slicing parameters rapidly without causing large variations in the BER (column 3, lines 56 – 58 – Hadjihassan et al. reference).

With respect to claim 32, all of the limitations of claim 29 have been addressed above. The Wiatrowski et al. reference does not teach a control signal that determines if the amount of current in said signal is increased or decreased. The Hadjihassan et al. reference teaches a control signal that determines if the amount of current in said signal is increased or decreased (column 5, line 61 – column 6, line 2). Thus it would have been obvious to one of ordinary skill in the art to have combined the references Wiatrowski et al. and Hadjihassan et al. to incorporate a control signal that determines if the amount of current in said signal is increased or decreased. The motivation for a control signal that determines if the amount of current in said signal is increased or decreased is to approach optimum values of the slicing parameters rapidly without causing large variations in the BER (column 3, lines 56 – 58 – Hadjihassan et al. reference).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Enam Ahmed whose telephone number is 571-270-1729. The examiner can normally be reached on Mon-Fri from 8:30 A.M. to 5:30 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques, can be reached on 571-272-6962.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EA

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7/2/07

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